REMARKS/ARGUMENTS

A new title has been provided as suggested by the Examiner.

Claims 1-24 are pending in the present application. Claim 18 was amended. No claims were added or canceled. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the following comments.

I. Double Patenting

The Examiner has provisionally rejected claims 1, 3-6, 8, 11, 13-15, 18 and 20-22 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3, 6-7, 9, 12-14, 17-20 , and 23 of copending Application No. 10/806,866.

The Examiner states:

> Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 3-6, 8, 11, 13-15, 18, and 20-22 of the instant application are an obvious modification of claims 1-3, 6-7, 9, 12-14, 17-20, and 23 of copending application.
>
> This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Office Action dated September 19, 2006, page 4.

Although Applicants do not acknowledge that claims of the present application and claims of copending application 10/806,866 are not patentably distinct from one another, a terminal disclaimer is submitted herewith in order to expedite prosecution. Withdrawal of the provisional rejection of claims 1, 3-6, 8, 11, 13-15, 18 and 20-22 is, accordingly, respectfully requested.

Therefore, the provisional rejection of claims 1, 3-6, 8, 11, 13-15, 18 and 20-22 on the grounds of double patenting has been overcome.

II. 35 U.S.C. § 101

The Examiner has rejected claims 18-24 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> Claims 18-24 are not limited to tangible embodiments. In view of Applicant's disclosure, pg. 59, paragraph 1, the computer readable medium is not limited to tangible embodiments, instead being define as including both tangible embodiments (e.g. recordable-type media, such as a floppy disk, hard disk drive, a RAM, CD-ROMS, and DVD-ROMS) and intangible embodiments (e.g. transmission-type media, such as digital

and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions). As such, claims 18-24 are not limited to statutory subject matter and are therefore non-statutory.

Office Action dated September 19, 2006, pages 11-12.

Although Applicants believe claims 18-24 recite statutory subject matter and fully satisfy the requirements of 35 U.S.C. § 101 in their present form, in order to expedite prosecution, claim 18 has been amended to recite a "computer program product in a recordable-type computer readable medium". As noted by the Examiner, this language is fully supported in the present specification on page 59, lines 10-12 and covers tangible embodiments that clearly satisfy the requirements of 35 U.S.C. § 101.

Therefore, the rejection of claims 18-24 under 35 U.S.C. § 101 has been overcome.

III. 35 U.S.C. § 103, Obviousness: Claims 1-2, 5, 7-12, 15, 17-19, 22, and 24

The Examiner has rejected claims 1-2, 5, 7-12, 15, 17-19, 22, and 24 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* et al., U.S. Patent No. 6,381,679 B1 (hereinafter "*Matsubara*") in view of Anonymously Disclosed, Method for the Dynamic Prediction of Nonsequential Memory Accesses, September 25, 2002 (hereinafter "*Anon*"). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> **As per claims 1 and 18,** Matsubara discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:
>
> responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22). *It should be noted that computer program product in claims 18-24 executes the exact same functions as the methods in claims 1- 7. Therefore, any references that teach claims 1-7 also teach the corresponding claims 18-24. It should also be noted that the "indication bits (i.e. PF bits)" are analogous to the "prefetch indicator" and the "CPU 21" is analogous to the "processing unit."*
>
> and responsive to the prefetch indicator being associated with the instruction, selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22).
>
> Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator.
>
> Anon discloses a pointer to a data structure identified by the prefetch indicator. (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *It should be noted that the "dynamic prefetch pointer" is analogous to the "pointer to a data structure."*
>
> Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

Therefore, it would have been obvious to combine Matsubara and Anon for the benefit of obtaining the invention as specified in claims 1 and 18.

Office Action dated September 19, 2006, pages 12-14.

Claim 1 is as follows:

1. A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction; and

responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor.

Applicants respectfully submit that neither *Matsubara*, nor *Anon*, nor their combination teaches or suggests "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction" or "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1.

In rejecting the claims, the Examiner refers specifically to col. 5, lines 1-10; col. 6, lines 35-42; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22 of *Matsubara* as disclosing "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction". Applicants respectfully disagree. The recitations referred to by the Examiner are reproduced below for the Examiner's convenience:

In an information processing unit having a software prefetch instruction for transferring an operation data to be used for an operation from a main memory to a cache prior to the execution of the operation, the above-described object of the present invention can be achieved by providing one or a plurality of indication bits for indicating the content of a prefetch operation. The indication bits are included in either an operation code or an operand address of the software prefetch instruction. The type or content of the prefetch operation performed is based on the indication bits.

Matsubara, col. 5, lines 1-10.

In the format of an operation address of a software prefetch instruction shown in FIG. 1, the lower five bits of the operation address are not necessary for a software prefetch instruction since the block size of the operation address is 32 B. Accordingly, the lower five bits are used as bits for indicating the content of a prefetch operation

(hereinafter to be referred to as Prefetch (PF) bits) in one embodiment of the present invention.

Matsubara, col. 6, lines 35-42.

> The operation of a software prefetch instruction in the information processing unit according to one embodiment of the present invention shown in FIG. **2** will be explained next. The information processing unit shown in the drawing to which the present invention is applied is an information processing unit having a cache structure of two hierarchical levels which is the same as the structure of the conventional technique shown in FIG. **7**.

Matsubara, col. 7, lines 10-20.

Nowhere in the above recitations or anywhere in *Matsubara* is there any disclosure or suggestion of "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction". *Matsubara* describes that one or a plurality of "indication bits" can be provided in either an operation code or in an operand address of a software prefetch instruction for indicating the content of a prefetch operation. As described in Col. 5, lines 11-24 of *Matsubara*, such indication bits can indicate such things as at least one of a hierarchical level of a cache to which the operation data is to be prefetched and a quantity of the operation data to be prefetched. In *Matsubara*, a value of the indication bits indicates the operation to be performed.

Nowhere, however, does *Matsubara* disclose or suggest that a determination is made "whether a prefetch indicator is associated with the instruction" or that such a determination is made by a processor "responsive to loading an instruction in the code into a cache" as required by claim 1.

Matsubara also does not disclose or suggest "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1. Although *Matsubara* may disclose prefetching data in accordance with a value of a software prefetch instruction, this is not the same as selectively prefetching a pointer to a data structure identified by a prefetch indicator "responsive to the prefetch indicator being associated with the instruction".

The Examiner acknowledges that *Matsubara* fails to disclose a pointer to a data structure identified by a prefetch indicator, and cites *Anon* as disclosing a pointer to a data structure. *Anon*, however, does not supply the deficiencies in *Matsubara* described above. *Matsubara* in view of *Anon* still fails to teach or suggest "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction" or "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1. Claim

1, accordingly, is not obvious over *Matsubara* in view of *Anon*, and patentably distinguishes over the references in its present form.

Independent claims 8, 11 and 18 patentably distinguish over *Matsubara* in view of *Anon* for similar reasons as discussed above with respect to claim 1.

Claims 2, 5, 7, 9, 10, 12, 15, 17, 19, 22 and 24 depend from and further restrict one of claims 1, 8, 11 and 18 and also patentably distinguish over *Matsubara* in view of *Anon* at least by virtue of their dependency.

Therefore, the rejection of claims 1-2, 5, 7-12, 15, 17-19, 22, and 24 under 35 U.S.C. § 103(a) has been overcome.

IV. 35 U.S.C. § 103, Obviousness: Claims 3, 13 and 20

The Examiner has rejected claims 3, 13, and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* in view of *Anon* as applied to claims 1 and 11 above, and in further view of IBM Technical Disclosure, Cache Miss Director – A Means of Prefetching Cache Missed Lines (hereinafter IBMTD). This rejection is respectfully traversed.

The Examiner states:

> **As per claims 3 and 20,** the combination of Matsubara/Anon discloses all the limitations of claims 3 and 20 except determining whether outstanding cache misses are present;
>
> and prefetching the data if a number of outstanding cache misses are less than a threshold.
>
> IBMTD discloses determining whether outstanding cache misses are present (Discourse Text, lines 13-14); *It should be noted that the "demand miss" analogous to the "cache miss."*
>
> and prefetching the data if a number of outstanding cache misses are less than a threshold (Discourse Text, lines 14-17). *It should be noted that this limitation contains language that suggests or makes optional but does not require steps to be performed or does not limit the claim to a particular structure and therefore does not limit the scope of a claim. Thus, simply "prefetching the data" is disclosed because the optionally recited parts of this limitation are not required to be taught by the Office. See MPEP §2106, Section II(C)). It should also be noted that "anticipatory cache misses" are analogous to "prefetching data."*
>
> The combination of Matsubara/Anon and IBMTD are analogous art because they are from the same field of endeavor, that being prefetching memory systems.
>
> At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's Cache Miss Directory (CMD) within Matsubara/Anon's information processing system.
>
> The motivation for doing so would have been to get the lines into the cache before a demand miss occurs for them, thus, reducing processing delays (IBMTD, Discourse Text, lines 2-3 and 19-20).

Therefore, it would have been obvious to combine Matsubara, Anon, and IBMTD for the benefit of obtaining the invention as specified in claims 3 and 20.

Office Action dated September 19, 2006, pages 18-19.

Claims 3, 13 and 20 depend from and further restrict one of claims 1, 11 and 18. IBMTD does not supply the deficiencies in *Matsubara* and *Anon* as described above. Claims 3, 13 and 20, accordingly, are patentable over the references, at least by virtue of their dependency.

In addition, Applicants respectfully disagree with the Examiner's assertion that claims 3 and 20 contain language that suggests or makes optional, but does not require, steps to be performed or does not limit the claim to a particular structure. Claims 3 and 13 positively recite "prefetching the data if a number of outstanding cache misses are less than a threshold". This is a positively recited limitation that cannot be simply ignored in rejecting the claims. IBMTD does not disclose this limitation, and claims 3, 13 and 20 patentably distinguish over the cited art in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 3, 13, and 20 under 35 U.S.C. § 103(a) has been overcome.

V. 35 U.S.C. § 103, Obviousness: Claims 4, 6, 16, 21 and 23

The Examiner has rejected claims 4, 6, 16, 21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* in view of *Anon* as applied to claims 1 and 11 above, and in further view of *Malik*, U.S. Patent No. 6,687,794 B2. This rejection is respectfully traversed.

Claims 4, 6, 16, 21, and 23 depend from and further restrict one of claims 1, 11 and 18. *Malik* does not supply the deficiencies in *Matsubara* and *Anon* as described above. Claims 4, 6, 16, 21 and 23, accordingly, patentably distinguish over the references and are allowable in their present form, at least by virtue of their dependency.

With respect to claims 4 and 21, in particular, Applicants again disagree that these claims recite optional language that need not be considered in examining the claims. The claims recite positive limitations of "determining whether to replace cache lines" and "prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold". *Malik* does not disclose the subject matter of claims 4 and 21 and these claims patentably distinguish over the cited art and are allowable in their own right as well as by virtue of their dependency.

Therefore, the rejection of claims 4, 6, 16, 21, and 23 under 35 U.S.C. § 103(a) has been overcome.

VI. Conclusion

For at least all the above reasons, Applicants believe that the subject application is patentable over the cited references and is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

/Gerald H. Glanzman/

Gerald H. Glanzman
Reg. No. 25,035
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants